

REMARKS

In response to the Office Action of June 15, 2006, Applicant (1) requests withdrawal of the finality of that Office Action and (2) requests reconsideration.

“Finality” is premature

Claims 1, 4-5 and 7-10 have been rejected over a new reference, Butler. Despite the new ground of rejection, the Examiner has made the Office Action final, stating that “Applicant’s amendment necessitated the new ground(s) of rejection presented in this Office Action.”

However, Applicant’s response of March 28, 2006 did not amend any claims.

Inasmuch as there were no amendments to any of the independent claims, the new ground of rejection is not necessitated by Applicant’s immediately preceding response and finality is therefore improper when a new ground of rejection is presented for the first time in the outstanding Office Action. Accordingly, the “final” status of the Office Action should be withdrawn.

There was, unfortunately, an error in the previous Amendment, which the Office apparently did not detect and did not bring to Applicant’s attention. It was entirely inadvertent. However, claims 1 and 5 had been amended in an October 5, 2005 Amendment, but the changes to those claims were not preserved in the March 28, 2006 Amendment. Accordingly, Applicant has repeated above the claims as they should have been presented in the March 28, 2006 Amendment – i.e., including the October 5, 2005 amendments and marked a previously presented.

Request for Reconsideration

Claim 1, as previously amended, is drawn to a memory cell “consisting essentially of” three elements, a charge storage element, a one-transistor switch and a one-transistor gain element. The gain element is further indicated as “consisting essentially of” a FET (1) having certain connections and (2) being symmetrical with respect to its second and third terminals.

Contrary to the Office Action, Butler does not anticipate claims 1. Butler shows, in addition to his FET T2, a third FET T3 and it is only *through T3* that T2 is connected to the second data line. Such a connection is precluded by the limitation in claims 1 that the gain element is one “consisting essentially of” a FET One, not two. (“Consisting essentially of” is substantially closed.) Moreover, contrary to the Office Action, there is no disclosure in Butler of the FET T2 being symmetrical with respect to the second and third terminals. The Examiner does not even suggest anywhere in the Butler disclosure that there is any such teaching. Manifestly, one cannot determine from FIG. 4A of Butler that transistor T2 employs a geometrically or electrically symmetrical structure. The Examiner is entirely speculating in that respect. Speculation, however, may not be the basis for a proper anticipation rejection. The reference must clearly teach the claimed invention. It does not.

Claim 5 likewise distinguishes over the reference.

Accordingly, the rejection should be withdrawn. There is simply no disclosure in Butler of the claimed invention and the Examiner reads into Butler limitations taught only by Applicant.

Serial No.: 10/648,939
Conf. No.: 5934

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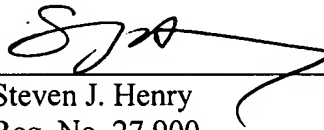
Art Unit: 2824

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,



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Docket No.: A0312.70480 US00
Date: September 15, 2006

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